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APPLICATION FOR LETTERS PATENT

for

**DEVICE AND METHOD FOR ISOLATING
A SHORT-CIRCUITED INTEGRATED CIRCUIT (IC)
FROM OTHER ICs ON A SEMICONDUCTOR WAFER**

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TITLE OF THE INVENTION

DEVICE AND METHOD FOR ISOLATING A SHORT-CIRCUITED INTEGRATED CIRCUIT (IC) FROM OTHER ICs ON A SEMICONDUCTOR WAFER

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application is a continuation of application Serial No. 10/218,279, filed August 13, 2002, pending, which is a continuation of application Serial No. 09/944,509, filed August 30, 2001, now U.S. Patent 6,452,415, issued September 17, 2002, which is a continuation of application Serial No. 09/083,819, filed May 22, 1998, now U.S. Patent 6,313,658, issued November 6, 2001.

BACKGROUND OF THE INVENTION

[0002] Field of the Invention: This invention relates in general to integrated circuits (ICs) fabricated on semiconductor wafers and, more specifically, to devices and methods for isolating a short-circuited IC from other ICs on a semiconductor wafer so that, for example, probe testing may proceed on the other ICs on the wafer despite the presence of the short-circuited IC.

[0003] State of the Art: As shown in FIG. 1, integrated circuits (ICs) 10 are small electronic circuits formed on the surface of a wafer 12 of semiconductor material, such as silicon, in an IC manufacturing process referred to as "fabrication." Once fabricated, ICs 10 are electronically probed to evaluate a variety of their electronic characteristics. Probing typically involves positioning needle-like probes (not shown) onto bond pads 14 on the surfaces of ICs 10 to test the ICs 10 using various electronic signals supplied through the probes. As described in U.S. Patent Nos. 5,059,899 and 5,214,657 to Farnworth et al., in some cases, ICs 10 are tested using test probes that contact probe pads 16 positioned on the surface of a semiconductor wafer 12 rather than, or in addition to, contacting bond pads 14 on the ICs 10.

[0004] Sometimes shorts develop in some of the ICs 10 on a semiconductor wafer 12 as a result of fabrication errors. These shorts can interfere with the probe testing described above in

a variety of ways. For example, in some instances, a supply voltage V_{CC} , provided to ICs 10 on a wafer 12 through probes contacting bond pads 14 on the ICs 10 or probe pads 16 on the wafer 12, may be shorted to ground through one of the ICs 10. As a result, over-current protection circuitry, such as a fuse, present in testing equipment that provides the supply voltage V_{CC} to the probes, will likely “trip” the equipment off-line, causing a brief but significant delay in the manufacturing of ICs 10 while the equipment is reset. In addition, such a V_{CC} -to-ground short in an IC 10 may make the entire wafer 12 untestable until the IC 10 with the short is identified and either repaired or disconnected, which involves a separate manual process that can cause additional delays in the manufacturing process.

[0005] In other instances, a test signal V_{TEST} supplied to a group of ICs 10 on a semiconductor wafer 12 through a probe pad 16 on the wafer 12 may be distorted for all of the ICs 10 in the group by, for example, a V_{TEST} -to-ground or a V_{TEST} -to- V_{CC} short in one of the ICs 10 in the group. This distortion may interfere with probe testing of all of the ICs 10 in the group, and may require that the IC 10 with the short be manually identified and repaired or disconnected before the ICs 10 in the group can be successfully probe tested.

[0006] Therefore, there is a need in the art for a device and method for isolating a short-circuited IC on a semiconductor wafer from other ICs on the wafer. Preferably, such a device and method should isolate a short-circuited IC before the IC interferes with probe testing of other ICs so the probe testing can continue uninterrupted.

BRIEF SUMMARY OF THE INVENTION

[0007] An inventive device for isolating a short-circuited integrated circuit (IC) from other ICs formed on the surface of a semiconductor wafer that are interconnected with the short-circuited IC includes control circuitry within the short-circuited IC for sensing the short circuit. The control circuitry may sense the short circuit in a variety of ways, including sensing excessive current drawn by the short-circuited IC, and sensing an abnormally low or high voltage within the short-circuited IC. Switching circuitry also within the short-circuited IC selectively isolates the short-circuited IC from the other ICs on the wafer in response to the control circuitry sensing the

short circuit. As a result, if the wafer is under probe test, for example, testing can continue uninterrupted on the other ICs while the short-circuited IC is isolated.

[0008] Further embodiments of the present invention are directed to an IC including the control and switching circuitry described above, a semiconductor wafer including many of these ICs, and an electronic system, such as a computer system, including at least one of these ICs.

[0009] In an inventive method for testing ICs formed on the surface of a semiconductor wafer, control circuitry is provided in the ICs for sensing shorts in the ICs. The ICs are then tested, and if the control circuitry in one of the ICs senses a short, the short-circuiting IC is automatically switchably isolated from the other ICs.

BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWINGS

[0010] FIG. 1 is a prior art top view of a conventional semiconductor wafer showing interconnected integrated circuits (ICs) formed on the surface of the wafer;

[0011] FIG. 2 is a block diagram and a schematic of an IC including circuitry for isolating a short-circuiting circuit internal to the IC from a supply voltage V_{CC} bond pad on the IC in accordance with the present invention;

[0012] FIG. 3 is a top view of a semiconductor wafer including interconnected ICs formed on its surface that are identical to the IC shown in FIG. 2;

[0013] FIG. 4 is a block diagram of an electronic system including the IC of FIG. 2;

[0014] FIG. 5 is a block diagram and a schematic of an IC including an alternative embodiment of circuitry for isolating a short-circuiting circuit internal to the IC from a supply voltage V_{CC} bond pad on the IC in accordance with the present invention;

[0015] FIG. 6 is a block diagram and a schematic of another alternative embodiment of circuitry for isolating a short-circuiting circuit internal to an IC from a supply voltage V_{CC} bond pad on the IC in accordance with the present invention; and

[0016] FIG. 7 is a block diagram and a schematic of still another alternative embodiment of circuitry for isolating a short-circuiting circuit internal to an IC from a supply voltage V_{CC} bond pad on the IC in accordance with the present invention.

DETAILED DESCRIPTION OF THE INVENTION

[0017] As shown in FIG. 2, an integrated circuit (IC) 20 in accordance with the present invention includes control circuitry 22 for sensing a short in a circuit 24 internal to the IC 20 and switching circuitry 26 for isolating the internal circuit 24 from a supply voltage V_{CC} bond pad 28 on the IC 20 in response to the control circuitry 22 sensing the short. By isolating the short-circuited internal circuit 24 from the supply voltage V_{CC} bond pad 28, the present invention can prevent the short from “tripping” probe test equipment (not shown) supplying the supply voltage V_{CC} to a semiconductor wafer (not shown) during probe testing of the wafer.

[0018] It should be understood that the IC may comprise any IC, including, for example, a Dynamic Random Access Memory (DRAM) IC and a Static RAM (SRAM) IC. It should also be understood that although the control circuitry and switching circuitry will be described with respect to specific circuitry, the present invention includes within its scope any control circuitry and any switching circuitry capable of performing the functions as described. Also, although the control circuitry will be described as sensing the short in the internal circuit by sensing excess current drawn by the internal circuit, the control circuitry may instead be constructed to sense abnormally high or low voltages within the internal circuit indicative of a short circuit. Further, it should be understood that while the present invention is considered most applicable to probe testing, its applicability is not limited to probe testing. In addition, it should be understood that the present invention can be used to isolate short-circuiting internal circuitry of an IC from a wide variety of circuitry external to the IC, and thus is not limited to isolating internal circuitry from a supply voltage V_{CC} bond pad.

[0019] Under normal probe testing conditions of the IC 20, when a short circuit does not exist in the internal circuit 24, a ground voltage V_{SS} applied at the gate of a switching PMOS transistor 32 through a large resistance device 34 (e.g., more than 1 MΩ) turns the switching PMOS transistor 32 on. The ground voltage V_{SS} is also applied at the input of an inverter 36, which then outputs a high voltage at the gate of a hysteresis PMOS transistor 38, causing the hysteresis PMOS transistor 38 to be off. Because the switching PMOS transistor 32 is on, the supply voltage V_{CC} applied at the bond pad 28 causes a current I to flow through a sensing resistance device 40 and the switching PMOS transistor 32 to the internal circuit 24.

[0020] The amount of resistance R of the sensing resistance device 40 is selected so that, under normal probe testing conditions, the current I drawn by the internal circuit 24 causes a voltage drop V (equal to $I \times R$) across the sensing resistance device 40 that is less than the threshold voltage $|V_T|$ of a sensing PMOS transistor 42. As a result, the sensing PMOS transistor 42 is off.

[0021] When a short circuit (e.g., a short circuit to ground) does exist in the internal circuit 24, the internal circuit 24 rapidly draws excessive current I through the sensing resistance device 40, causing the voltage drop V across the sensing resistance device 40 to exceed the threshold voltage $|V_T|$ of the sensing PMOS transistor 42. As a result, the sensing PMOS transistor 42 turns on, thereby applying the supply voltage V_{CC} at the gate of the switching PMOS transistor 32 and at the input of the inverter 36. Application of the supply voltage V_{CC} at the input of the inverter 36 causes the inverter 36 to output a low voltage at the gate of the hysteresis PMOS transistor 38, thereby turning the hysteresis PMOS transistor 38 on and reinforcing application of the supply voltage V_{CC} at the gate of the switching PMOS transistor 32. This causes the switching PMOS transistor 32 to turn off, thereby interrupting the excessive current flow I and isolating the short-circuited internal circuit 24 from the bond pad 28.

[0022] Because the current flow I is interrupted, the voltage drop V across the sensing resistance device 40 drops to zero, causing the sensing PMOS transistor 42 to turn off. Despite this, the switching PMOS transistor 32 remains off, because feedback of the supply voltage V_{CC} from the drain of the hysteresis PMOS transistor 38 to the input of the inverter 36 causes the inverter 36 to continue to output a low voltage at the gate of the hysteresis PMOS transistor 38, thereby causing the hysteresis PMOS transistor 38 to remain on and to continue to apply the supply voltage V_{CC} to the gate of the switching PMOS transistor 32. The IC 20 remains in this state, with the short-circuited internal circuit 24 isolated from the bond pad 28, and hence from other ICs under test, by the switching PMOS transistor 32 until the supply voltage V_{CC} is no longer applied to the bond pad 28, at which point the control circuitry 22 is reset.

[0023] As shown in FIG. 3, multiple ICs 20 are formed and interconnected on the surface of a semiconductor wafer 50 in accordance with the present invention. As shown in FIG. 4, an electronic system 52, such as a computer system, includes an input device 54, an

output device 56, a processor 58, and a memory device 60 incorporating the IC 20 of FIGS. 2 and 3.

[0024] As shown in FIG. 5, an IC 70 in accordance with an alternative embodiment of the present invention includes a fuse 72 for sensing a short in a circuit 74 internal to the IC 70 and for isolating the internal circuit 74 from a supply voltage V_{CC} bond pad 78 on the IC 70 when excessive current is drawn by the short.

[0025] As shown in FIG. 6 in another alternative embodiment of the present invention, an IC 80 includes control circuitry 82 for sensing a short in a circuit 84 internal to the IC 80 and switching circuitry 86 for isolating the internal circuit 84 from a supply voltage V_{CC} bond pad 88 on the IC 80 in response to the control circuitry 82 sensing the short. By isolating the short-circuited internal circuit 84 from the supply voltage V_{CC} bond pad 88, the present invention can prevent the short from “tripping” probe test equipment (not shown) supplying the supply voltage V_{CC} to a semiconductor wafer (not shown) during probe testing of the wafer.

[0026] Under normal probe testing conditions of the IC 80, when a short circuit does not exist in the internal circuit 84, a series of biasing resistors 90, 92, and 94 biases the base 96 of a switching bipolar junction transistor (BJT) 98 at a voltage intermediate the supply voltage V_{CC} and a ground voltage V_{SS} so that the BJT 98 is on. A voltage taken from between the biasing resistors 92 and 94 and applied at the input of an inverter 100 causes the inverter 100 to output a high voltage to the gate of a hysteresis PMOS transistor 102, causing the hysteresis PMOS transistor 102 to be off. Because the switching BJT 98 is on, the supply voltage V_{CC} applied at the bond pad 88 causes a current I to flow through a resistor 104 and the BJT 98 to the internal circuit 84.

[0027] The amount of resistance R of the resistor 104 is selected so that, under normal probe testing conditions, the current I drawn by the internal circuit 84 causes a voltage drop V (equal to I×R) across the resistor 104 that is less than the threshold voltage |V_T| of a sensing PMOS transistor 106. As a result, the sensing PMOS transistor 106 is off.

[0028] When a short circuit (e.g., a short circuit to ground) does exist in the internal circuit 84, the internal circuit 84 rapidly draws excessive current I through the resistor 104, causing the voltage drop V across the resistor 104 to exceed the threshold voltage |V_T| of the

sensing PMOS transistor 106. As a result, the sensing PMOS transistor 106 turns on, thereby applying the supply voltage V_{CC} at the base of the switching BJT 98 and raising the voltage applied at the input to the inverter 100. The rising voltage at the input of the inverter 100 causes the inverter 100 to output a low voltage at the gate of the hysteresis PMOS transistor 102, thereby turning the hysteresis PMOS transistor 102 on and reinforcing application of the supply voltage V_{CC} at the base 96 of the switching BJT 98. This causes the switching BJT 98 to turn off, thereby interrupting the excessive current flow I and isolating the short-circuited internal circuit 84 from the bond pad 88.

[0029] Because the current flow I is interrupted, the voltage drop V across the resistor 104 drops to zero, causing the sensing PMOS transistor 106 to turn off. Despite this, the switching BJT 98 remains off, because the raised voltage at the input to the inverter 100 causes the inverter 100 to keep the hysteresis PMOS transistor 102 on, allowing the hysteresis PMOS transistor 102 to continue to apply the supply voltage V_{CC} to the base 96 of the BJT 98. The IC 80 remains in this state, with the short-circuited internal circuit 84 isolated from the bond pad 88, and hence from other ICs under test, by the switching BJT 98 until the supply voltage V_{CC} is no longer applied to the bond pad 88, at which point the control circuitry 82 is reset.

[0030] It should be understood that the switching BJT 98 may be implemented on the IC 80, as is shown in FIG. 6, in a BiCMOS configuration or, alternatively, may be implemented on a probe card contacting the bond pad 88 or between ICs on a semiconductor wafer.

[0031] As shown in FIG. 7 in still another alternative embodiment of the present invention, an IC 110 includes control circuitry 112 for sensing a short in a circuit 114 internal to the IC 110 and a micro-relay 116 for isolating the internal circuit 114 from a supply voltage V_{CC} bond pad 118 on the IC 110 in response to the control circuitry 112 sensing the short. By isolating the short-circuited internal circuit 114 from the supply voltage V_{CC} bond pad 118, the present invention can prevent the short from “tripping” probe test equipment (not shown) supplying the supply voltage V_{CC} to a semiconductor wafer (not shown) during probe testing of the wafer.

[0032] Under normal probe testing conditions of the IC 110, when a short circuit does not exist in the internal circuit 114, the control circuitry 112 senses no short in the internal

circuit 114, so it causes the micro-relay 116 to close and allow a current I to flow to the internal circuit 114.

[0033] When a short circuit (e.g., a short circuit to ground) does exist in the internal circuit 114, the internal circuit 114 rapidly draws excessive current I. The control circuitry 112 detects this excessive current I and, as a result, causes the micro-relay 116 to open, thereby isolating the internal circuit 114 from the bond pad 118. The control circuitry 112 remains in this state until reset by the voltage at the bond pad 118 dropping to zero and then rising again to the supply voltage V_{CC} .

[0034] It should be understood that the micro-relay may be created using silicon micro-machining techniques, and may comprise a capacitively or inductively controlled relay.

[0035] Although the present invention has been described with reference to particular embodiments, the invention is not limited to these described embodiments. For example, while the various steps of operating the inventive device, and hence the various steps of the inventive method, have been described as occurring in a particular order, it will be understood that these steps need not necessarily occur in the described order to fall within the scope of the present invention. Thus, the invention is limited only by the appended claims, which include within their scope all equivalent devices and methods that operate according to the principles of the invention as described.